CHAPTER 3

TECHNICAL MAINTENANCE INFORMATION

Section I. THEORY OF OPERATION

3-1. VARIABLE LIGHTING INSTRUMENT

By now you should be familiar with the mechanics of the VARI*LITE 1 (VL1) luminaire, and know how to calibrate and repair the various sub-assemblies. In this chapter we will describe some of the more arcane workings of the luminaire, primarily for the benefit of the electronics technician who may be called upon to repair electronic circuits not covered in chapter two.

So how does the console and control rack communicate with the VL1 luminaires? You know that each luminaire can be set to respond to one of 100 channels, and that the control rack sends commands over 96 of those channels. The control rack sends a signal over a two-conductor shielded pair. This is a balanced line signal in which the signal that appears on one wire is inverted on the other wire. Throughout the following discussion we will describe the Positive Data signal, keeping in mind the same things are happening in the Negative Data signal, but the polarity of the signal is reversed.

NOTE

> Refer to paragraph 3-11. Trouble With The Repeater for a discussion of how the control signal is transmitted through the repeater.

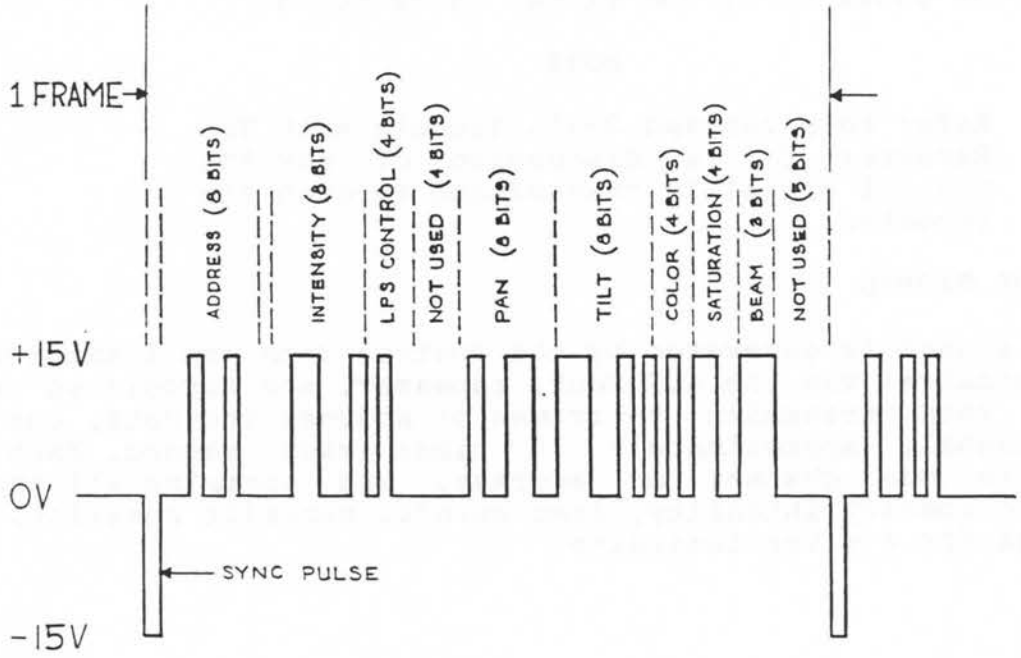
3-2. CONTROL SIGNAL

The control signal is generated by the control rack and transmitted to the VL1 luminaires via the ACS Rack, repeater, and associated cables. The control rack transmits 96 frames of address and data, one frame for each channel, approximately 18 times each second. Each frame corresponds to one channel or address, and contains all the data necessary to specify intensity, lamp on/off, pan/tilt position, color and beam size for a given luminaire.

3-2. CONTROL SIGNAL (CONT'D)

Each frame begins with a 10 micro-second (10 uS) sync pulse. Eight bits of address follow the sync pulse. Forty-eight (48) data bits follow the address information. Each bit is 10 uS wide. Each frame is about 580 uS wide, and is organized as follows:

- SYNC PULSE. A negative-going pulse 15 volts in amplitude, 10 uS wide.
- ADDRESS. Eight bits of information, organized as two Binary-Coded Decimal (BCD) digits. The first four bits are the Most Significant Digit (MSD). The second four bits are the Least Significant Digit (LSD). The first bit is the Most Significant Bit (MSB). The last bit is the Least Significant Bit (LSB). The BCD digits correspond to the two-digit thumbwheel address set on the luminaire.
- INTENSITY. Eight bits of data: two BCD digits; MSB first, LSB second. A 10 uS space separates the address and intensity data.
- LPS CONTROL. Four bits of data: LAMP ON, START-, CHASE OFF (not used), and FLASH (not used). Followed by four bits that are not used.
- PAN DATA. Eight bits: two BCD digits (MSD, LSD).
- TILT DATA. Eight bits: two BCD digits (MSD, LSD).



3-2. CONTROL SIGNAL (CONT'D)

- COLOR/SATURATION DATA. Four bits Color; four bits Saturation.
- BEAM SIZE DATA. Three bits of data followed by five bits not used.

The control rack transmits frames of data continuously. When you go to a new cue, the data is updated and transmitted. The control rack does not transmit the necessary data and then stop. The entire group of 96 frames takes about 55 milli-seconds (55 mS) to transmit. The lites receive sync pulses every 580 uS. If the sync pulses are not received, the lite closes its iris, but otherwise remains the same.

3-3. DATA RECEIVER

The operation of the Data Receiver circuit card assembly is best understood by considering three aspects of its internal functions: timing, data handling, and data conversion. The timing function breaks he frame into 580 parts, each 1 uS long. The data handling function screens the incoming sync, address, and data signals to eliminate noise or false data, and routes good data to the appropriate place. The data conversion function translates incoming data to control signals required by the servo circuits and Lamp Power Supply control circuit.

Timing

The frame is composed of 58 bit fields, each 10 uS wide. The first is the sync pulse field (bit field 00), followed by 8 fields of address bits, one blank field (bit field 09) separating the address from the data, and 48 fields for data bits. When a sync pulse appears at the Data/Sync Separator, the Sync Qualifier counts off 10 intervals of 1 uS each and, if the sync pulse is present for all 10 intervals, a Frame Enable signal (FRMEN-) is asserted. This enables the Clock Timing Counter and Data Bit Counter. The Clock Timing Counter counts off 10 intervals of 1 uS each during each of the remaining 57 bit fields. Several things happen sequentially during each of the 57 bit fields:

1. LATCH CLOCK (LCHCK). Asserted during interval 1, this signal clocks the Data Latches and combines with the data bit count to clock the Address Comparator's output flip-flop.

2. INTERNAL CLOCK (INTCK). Asserted during interval 2, this signal clocks the Data Bit Counter to increment the data bit count. By counting the data bits as they come in, the Receiver then "knows" whether the bit is address, Intensity data, Color data, Tilt data, or whatever.

3-3. DATA RECEIVER (CONT'D)

Timing (cont'd)

3. CLOCK RESET CLOCK (CRSCK). Asserted during interval 3, this signal combines with Frame End (FREND) to reset the Data Bit Counter. FREND is only asserted when the data bit count equals 57. So during interval 3 of bit field 57, the data bit count is reset to 0 to await the first address bit of the next frame.

4. SAMPLE A CLOCK (SMACK). Asserted during interval 4, this signal clocks a D flip-flop to load the first of five samples of the incoming data bit into the Data Sampling logic.

5. SAMPLE B CLOCK (SMBCK) -- SAMPLE E CLOCK (SMECK). Asserted during intervals 5 thru 8 respectively, these signals clock four other D flip-flops to load four more samples of the incoming data bit into the Data Sampling Logic.

6. SHIFT REGISTER CLOCK (SHRCK). Asserted during interval 9, this signal clocks the Data Shift Register to load the output of the Data Sampling Logic into the register.

At the end of the ten intervals (0 thru 9), several things have been accomplished: the Data Bit Counter has been incremented so we know which bit this is; five samples of the data bit have been loaded and compared by the majority logic gate; and the resultant data bit has been shifted into the Data Shift Register and thereby placed on the internal data bus. During interval 0 of the next bit field, the new data bit appears at the Data Sampling Logic flip-flops, and the process starts over.

Data Handling

Within each frame, the Data Bit Counter determines what will be done with the data bits as they are received. During the first 4 uS for each bit field, clock signals increment counters and the resultant control signals configure the Address Comparator or Data Latches to receive data bytes from the Data Shift Register. During the next 5 uS, the Data Sampling Logic loads samples of the data bit to determine if the bit is HI or LO. In the final micro-second, the data bit is loaded into the Data Shift Register.

3-3. DATA RECEIVER (CONT'D)

Data Handling (cont'd)

When the last bit of an 8-bit byte has been shifted into the Data Shift Register, the data is then utilized during the first few microseconds of the next bit field. If address bits are in the Data Shift Register, the Data Bit Counter asserts Address Clock (ADRCK) to load the results of the comparison into a flip-flop. An entire 10 uS bit field is reserved as a blank to provide enough time for address processing to occur. If data bits are in the Data Shift Register, the necessary data latching is accomplished in the first 4 uS of the next bit field. The data processing is then completed before samples of the subsequent bit (MSB of the next byte) are taken.

Data Conversion

Digital-to analog converters with operational amplifier current-to-voltage converting output buffers are used to translate data bytes to control voltages. The converters circuits are configured differently to accomodate differing requirements.

The Intensity circuit converts an 8-bit byte to a 0-to-12 volt signal, where zero data equals zero volts. The Pan circuit converts an 8-bit byte to a +/-8 volt signal. The MSB is inverted prior to conversion so that zero data yields zero volts, and that corresponds to mid-position at the Pan mechanism. The Tilt circuit is configured similarly to the Pan circuit, except that the output is scaled down to +/-6 volts.

The Beam circuit only requires the three Most Significant Bits of the beam size byte to specify one of eight positions of the beam wheel. The Beam control voltage goes from 0-to-12 volts in seven steps. The color circuit converts an 8-bit byte to three control signals of 0-to-12 volts, and utilizes three PROMs to relate color data to filter wheel positions. Each PROM yields a 3-bit output and from this point on the circuits are identical to the beam circuit.

Circuit Diagram - Functional Groups

The schematic diagram for the Data Receiver is divided into functional groups. Refer to the diagram on pages 3-33 and 3-35 during the following discussion.

- MASTER CLOCK OSCILLATOR. Three gates of U7 and the 4 MHz crystal comprise the signal source for on-board timing circuits. The 4MHz output, CLK4M, is used to drive the divide-by-four and decade counters in the Sync Qualifier and Clock Timing Counter circuits.

- DATA/SYNC ISOLATOR/SEPARATOR. U1, a dual optical isolator, performs as a balanced line receiver and data/sync separator. One side of the isolator responds to data bits and generates the data input signal DTINP. The other side responds to sync pulses and generates the sync input signal SNCIN.